ABSTRACT OF THE DISCLOSURE

A multiple mode clock receiver including first and second input AC-coupled capacitors, first and second voltage dividers and a differential amplifier. The voltage dividers each include first and second junctions, respectively, coupled to the first and second AC-coupled capacitors, respectively. The differential amplifier has first and second inputs coupled to the first and second junctions, respectively, and an output providing an output clock signal that is aligned with an input clock signal provided through the AC-coupled capacitors. The multiple mode clock receiver is a single circuit that aligns the output clock signal to any one of multiple forms of input clock signals, including a sole single-ended clock signal, a single-ended clock signal with a corresponding reference signal, and a differential clock signal.